CLAIMS

1. A data processing apparatus on a single semiconductor substrate comprising:

a flash memory including a plurality of electrically rewritable nonvolatile memory cells each of which is constructed of a single transistor; and

a central processing unit,

wherein the central processing unit decodes a command supplied from outside of the data processing apparatus during a first operation mode for controlling the flash memory from the outside of the data processing apparatus so as to determine a process to be performed to the flash memory, and

wherein the central processing unit performs the process to the memory cell corresponding to an address supplied from the outside of the data processing apparatus.

2. A data processing apparatus according to claim 1,

wherein the command includes:

a program command for instructing a writing of data supplied from the outside of the data processing apparatus to the memory cell,

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a program verify command for instructing to verify whether or not the data has been written into the memory cell,

an erase command for instructing an erasure of data stored in the memory cell, and

an erase verify command for instructing to verify whether or not the data has been erased from the memory cell.

3. A data processing apparatus according to claim 2, further comprising:

a first external terminal to which the command is supplied in the first operation mode; and

a command latch circuit coupled to the first external terminal and latching therein the command in the first operation mode.

4. A data processing apparatus according to claim 3, further comprising:

a second external terminal to which the address is supplied in the first operation mode; and

an address latch circuit coupled to the second external terminal and latching therein the address in the first operation mode.

5. A data processing apparatus according to claim 4, further comprising:

a data latch circuit for latching therein the data in the first operation mode.

6. A data processing apparatus according to claim 5, further comprising:

a command flag coupled to the command latch circuit and indicating whether or not the command has been written in the command latch circuit; and

a data flag coupled to the data latch circuit and indicating whether or not data has been written in the data latch circuit,

wherein the data latch circuit is coupled to the first external terminal, and

wherein the data latch circuit latches the data when the command flag indicates that the command has been written in the command latch circuit.

7. A data processing apparatus according to claim 6,

wherein the central processing unit decodes the command in response to a command flag indicating that the command has been written in the command latch circuit.

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8. A data processing apparatus according to claim 7,

wherein the command further includes a read command for instructing a reading of data from the memory cell according to the address in the first operation mode, and

wherein the data processing apparatus further comprises:

an internal bus coupled to the central processing unit, to the flash memory, to the data latch circuit, to the command latch circuit, and to the address latch circuit;

a gate circuit provided in the internal bus, the gate circuit selectively establishing:

a first state in which the command latch circuit, the address latch circuit and the data latch circuit are coupled to the flash memory and the central processing unit, and

a second state in which the command latch circuit, the address latch circuit and the data latch circuit are coupled to the flash memory but not to the central processing unit; and

a command decoder coupled to the command latch circuit and providing a control signal to the gate circuit so as to bring the gate circuit into the second state when the command decoder decodes the read command in the first operation mode.

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9. A data processing apparatus according to claim 7, further comprising:

a control register having control bits for indicating processes to be performed to the flash memory, wherein the central processing unit writes data into one of the control bits in accordance with the decoding result of the command during the first operation mode.

10. A data processing apparatus according to claim 2,

wherein the flash memory includes a plurality of memory blocks each of which is a unit for a simultaneous erasure.

11. A data processing apparatus according to claim 10,

wherein each memory block includes memory cells each having a control electrode coupled to a word line, a first main electrode coupled to a data line and a second main electrode coupled to a source line, and

wherein each of the memory blocks includes one common source line, at least one word line and at least one data line, the ones of the memory cells coupled to the one word line or the one data line in each memory

block being coupled to the common source line of that memory block so that each memory block forms a unit for simultaneous erasure.

12. A data processing apparatus according to claim 10,

wherein the plurality of memory blocks in the flash memory have mutually different storage capacities.

13. A data processing apparatus according to claim 10,

wherein the data processing apparatus further has a second operation mode for controlling a writing and an erasing of data to and from the flash memory, and

wherein the central processing unit generates an address for the flash memory in the second operation mode.

14. A data processing apparatus according to claim 13, further comprising:

a control register having control bits for indicating processes to be performed to the flash memory, wherein the central processing unit writes data into one of the control bits in accordance with the decoding result of the command during the first and second operation modes, and

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an erase block designation register having bits for designating one or more memory blocks to be erased, wherein the central processing unit writes data into one or more bits which corresponds to the memory blocks to be erased during the second operation mode.

15. A data processing apparatus according to claim 1,

wherein each memory cell has a control electrode coupled to a word line, a floating gate, a first main electrode coupled to a data line and a second main electrode coupled to a source line.

16. A data processing apparatus on a semiconductor integrated circuit device comprising:

a simultaneous erase type EEPROM; and

a central processing unit,

wherein the central processing unit is responsive to a command supplied from outside of the data processing apparatus and performs a process instructed by the command to the simultaneous erase type EEPROM by executing an erase control program and/or a write control program during a first operation mode for controlling an operation of the simultaneous erase type EEPROM from the outside of the data processing apparatus.

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17. A data processing apparatus acocrding to claim 16,

wherein the data processing apparatus further has a second operation mode for an erasing and/or a writing of data from or to the simultaneous erase type EEPROM,

wherein the central processing unit generates an address to be supplied to the simultaneous erase type EEPROM during the second operation mode, and

wherein an address to be applied to the simultaneous erase type EEPROM is supplied from the outside of the data processing apparatus during the first operation mode.

18. A data processing apparatus according to claim 16,

wherein the command includes:

a program command for instructing a writing of data supplied from the outside of the data processing apparatus to a memory cell of the simultaneous erase type EEPROM,

a program verify command for instructing to verify whether or not the data has been written into the memory cell,

an erase command for instructing an erasure of data stored in the memory cell, and

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an erase verify command for instructing to verify whether or not the data has been erased from the memory cell.

19. A data processing apparatus according to claim 16, further comprising:

a first external terminal to which the command is supplied in the first operation mode; and

a command latch circuit coupled to the first external terminal and latching therein the command in the first operation mode.

20. A data processing apparatus according to claim 19, further comprising:

a second external terminal to which the address is supplied in the first operation mode; and

an address latch circuit coupled to the second external terminal and latching therein the address in the first operation mode.

21. A data processing apparatus according to claim 20, further comprising:

a data latch circuit for latching the data in the first operation mode.

22. A data processing apparatus according to claim 21, further comprising:

a command flag coupled to the command latch circuit and indicating whether or not the command has been written in the command latch circuit; and

a data flag coupled to the data latch circuit and indicating whether or not data has been written in the data latch circuit,

wherein the data latch circuit is coupled to the first external terminal, and

wherein the data latch circuit latches the data when the command flag indicates that the command has been written in the command latch circuit.

23. A data processing apparatus according to claim 22,

wherein the central processing unit decodes the command in response to the command flag indicating that the command has been written in the command latch circuit.

24. A data processing apparatus according to claim 23,

wherein the command further includes a read command for instructing a reading of data from the memory cell according to the address in the first operation mode, and

wherein the data processing apparatus further comprises:

an internal bus coupled to the central processing unit, to the flash memory, to the data latch circuit, to the command latch circuit, and to the address latch circuit;

a gate circuit selectively establishing:

a first state in which the command latch circuit, the address latch circuit and the data latch circuit are coupled to the simultaneous erase type EEPROM and the central processing unit,

and

a second state in which the command latch circuit, the address latch circuit and the data latch circuit are coupled to the simultaneous erase type EEPROM but not to the central processing unit; and

a command decoder coupled to the command latch circuit and providing a control signal to the gate circuit so as to bring the gate circuit into the second state when the command decoder decodes the read command in the first operation mode.

25. A data processing apparatus according to claim 19, further comprising:

a control register having control bits for indicating processes to be performed to the simultaneous

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erase type EEPROM, wherein the central processing unit writes data into one of the control bits in accordance with the decoding result of the command during the first operation mode.

26. A data processing apparatus according to claim 17,

wherein the simultaneous erase type EEPROM includes a plurality of memory blocks each of which is a unit for a simultaneous erasure.

27. A data processing apparatus according to claim 26,

wherein each memory block includes memory cells each having a control electrode coupled to a word line, a floating gate, a first main electrode coupled to a data line and a second main electrode coupled to a source line, and

wherein each of the memory blocks includes one common source line, at least one word line and at least one data line, the memory cells coupled to the one word line or the one data line in each memory block being coupled to the common source line of that memory block so that each memory block forms the unit for simultaneous erasure.

28. A data processing apparatus according to claim 26,

wherein the plurality of memory blocks have mutually different storage capacities.

29. A data processing apparatus according to claim 26,

wherein the data processing apparatus further has a second operation mode for controlling a writing and an erasing of data to and from the flash memory, and

wherein the central processing unit generates an address for the flash memory in the second operation mode, and

wherein the data processing apparatus further comprises:

a control register having control bits for indicating processes to be performed to the simultaneous erase type EEPROM, wherein the central processing unit writes data into one of the control bits in accordance with the decoding result of the command during the first and second operation modes, and

an erase block designation register having bits for designating one or more memory blocks to be erased, wherein the central processing unit writes data into one or more bits which corresponds to one or more memory blocks to be erased during the second operation mode.

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30. A data processing apparatus according to claim 16,

wherein the simultaneous erase type EEPROM includes a plurality of memory cells each of which has a control electrode coupled to a word line, a floating gate, a first main electrode coupled to a data line and a second main electrode coupled to a source line.

31. A data processing apparatus acocrding to claim 16, further comprising:

a command decoder coupled to receive the command and providing a control in the first operation mode.

32. A data processing apparatus on a single semiconductor substrate, comprising:

an electrically erasable and programmable nonvolatile flash memory;

a central processing unit; and

a latch circuit for latching a command asynchronously supplied from outside of the data processing apparatus during an operation mode for controlling an operation of the flash memory from the outside of the data processing apparatus,

wherein the central processing unit is responsive to the command latched in the latch circuit and performs a process instructed by the command to the flash memory.

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33. A data processing apparatus acocrding to claim 32,

wherein the flash memory includes a plurality of nonvolatile memory cells each of which has:

a source region and a drain region formed in the semiconductor substrate, an insulating film on a surface of the semiconductor substrate above a spacing between the source and the drain region,

a floating gate on the insulating film,

an oxide film on the floating gate, and

a control gate on the oxide film.

34. A data processing apparatus acocrding to claim 32,

wherein the command includes:

a program command for instructing to write data supplied from the outside of the data processing apparatus to a memory cell of the flash memory,

a program verify command for instructing to verify whether or not the data has been written into the memory cell,

an erase command for instructing to erase data stored in the memory cell, and

an erase verify command for instructing to verify whether or not the data has been erased from the memory cell.

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35. A data processing apparatus according to claim 33, further comprising:

a command decoder coupled to the command latch circuit for decoding the command in the operation mode.

36. A data processing apparatus acocrding to claim 33, further comprising:

an address latch circuit for latching therein an address supplied from the outside of the data processing apparatus in the operation mode; and

a data latch circuit for latching therein data which is to be written to the memory cell and which is supplied from the outside of the data processing apparatus in the operation mode.

37. A data processing apparatus acocrding to claim 34, further comprising:

a control register having control bits for indicating processes to be performed to the flash memory, wherein the central processing unit writes data into one of the control bits in accordance with the command during the operation mode.

38. A data processing apparatus on a semiconductor substrate, comprising:

a flash memory including electrically erasable and programmable nonvolatile memory cells;

a central processing unit; and

a memory which stores an erase and a write control program which are to be executed by the central processing unit in an external write operation mode in which the flash memory is made erasable and writable in accordance with a command supplied from outside of the data processing apparatus, and

wherein the central processing unit is responsive to the command and executes the erase and/or the write control program in the memory so as to perform a process instructed by the command to the flash memory.

39. A data processing apparatus according to claim 38, wherein the command includes:

a program command for instructing a writing of data supplied from the outside of the data processing apparatus to a memory cell of the flash memory,

a program verify command for instructing to verify whether or not the data has been written into the memory cell,

an erase command for instructing an erasure of data stored in the memory cell, and

an erase verify command for instructing to verify whether or not the data has been erased from the memory cell.

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40. A data processing apparatus according to claim 39, further comprising:

a command decoder coupled to receive the command and for decoding the command in the external write operation mode.

41. A data processing apparatus on a single semiconductor substrate, comprising:

a central processing unit;

an electrically erasable and programmable nonvolatile flash memory; and

wherein the apparatus has an external write operation mode in which the flash memory is erasable and writable in accordance with commands supplied from outside of the apparatus, and further comprises:

a command latch circuit for latching the command in the external write operation mode;

a command analysis circuit for analyzing the command latched in the command latch circuit to provide control signals according to an analyzing result of the command; and

a sequence control circuit for controlling a sequence of erasing and/or writing the flash memory in accordance with the control signals.

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